2.488 Gb/s SONET Multiplexer/Demultiplexer with Frame Detection Capability

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Abstract—In a gigabit/second transmission system, the portion of circuitry operating at the line rate is usually kept to the simplest form in order to maximize the circuit performance. For instance, the high-speed multiplexer (mux) and demultiplexer (demux) perform only the bit interleaving and deinterleaving functions, and the frame detection function is performed at low speed by a separate framing circuit. Such an architecture, however, requires close feedback interactions between the high-speed demultiplexer and the low-speed framing ciruit in order to achieve proper frame synchronization. For a gigabit/second SONET (synchronous optical network) transmission system, this could significantly increase the system design complexity. This paper describes a novel scheme that allows a demultiplexer, a byte aligner, and a frame detection circuit all integrated on one chip without compromising the demultiplexer's performance. A research prototype integrated circuit (IC) that incorporates this scheme was designed to operate at speeds up to the SONET STS-48 (synchronous transport signal level 48) rate of 2.488 Gb/s. The IC is implemented in GaAs enhancement/depletion mode MESFET technology, and it performs 1:8 demultiplexing, byte alignment, and SONET frame detection functions. A separate IC that performs 8:1 multiplexing was also implemented using the same technology. The bit error rate test results show that the multiplexer and demultiplexer with frame detector can operate at 2.488 Gb/s with a bit error rate less than 1×10^{-14}. Both IC's were tested at data rates up to 3 Gb/s.

I. Introduction

SONET (synchronous optical network) is an international standard for synchronous optical transmission [1], [2]. It defines a set of standard rates, formats, interface parameters, multiplexing schemes, and OAM&P (operation, administration, maintenance, and provisioning) specifications.

In the North American SONET digital hierarchy, the basic modular signal is STS-1 (synchronous transport signal level 1) with a transmission bit rate of 51.84 Mb/s. The higher level signal, STS-N (synchronous transport signal level N), is formed by byte interleaving N STS-1 signals and has a bit rate equal to N times the signal rate of STS-1. At present, the highest signal level defined in the SONET digital hierarchy is the STS-48, with a line rate of 2.488 Gb/s. Each SONET (STS-N) signal is composed of 125 μs frames, and each frame consists of nine rows of $90N$ columns of 8-bit bytes, for a total of $810N$ bytes. Fig. 1 depicts the structure of the STS-N frame.

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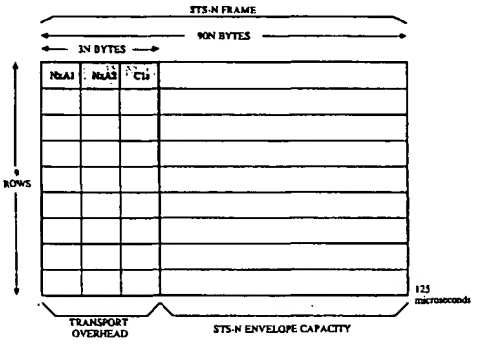

Fig. 1. SONET STS-N frame structure. A1 (11110110), A2 (00101000) are SONET framing bytes, and C1's are constituent STS-1s' channel identification numbers.

The first $3N$ columns of each frame are the transport overhead, and the remaining $87N$ columns are used to carry the information payloads (e.g., DS1, DS3, LAN, video and broadband ISDN services) and their path layer overhead [1]. The order of transmission is from left to right, row by row.

In order to receive and process the SONET signal, the SONET receiver must carefully identify and align with the incoming signal's bit, byte, and frame boundaries. The bit timing can be recovered by using a clock extraction circuit similar to the ones used in today's asynchronous lightwave systems. The byte and frame alignment, on the other hand, requires special circuit and system design in order to meet the new SONET framing requirements [3]. In this paper, we present a novel framing scheme which allows a high-speed (1:8) demultiplexer, a byte aligner, and a frame detection circuit all integrated on one chip without compromising the high-speed demultiplexer's performance. This approach greatly simplifies the system design, and it also eliminates the need for passing critical timing information on board from the low-speed framing circuit to the high-speed demux during a frame realignment process. A research prototype IC that incorporates this scheme was designed and implemented using the GaAs enhancement/depletion mode MESFET (metal semiconductor field effect transistor) technology. A separate IC that performs the high-speed 8:1 multiplexing was also implemented using the same technology. Both IC's operate at data rates up to 3 Gb/s. In the following

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section, we review the conventional high-speed and low-speed framing approaches used in today's digital transmission equipment. In Section III, we present the new SONET demultiplexing and frame detection scheme. In Section IV, we discuss the performance considerations of the SONET framing strategy, and in Section V, we describe the high-speed multiplexer design. The circuit implementation and test results are discussed in Section VI, and the conclusions of this paper are given in Section VII.

II. Conventional Framing Approaches

There are two basic framing methods employed by digital lightwave transmission systems, namely, the high-speed framing approach and the low-speed framing approach [4], [5]. Figs. 2 and 3 illustrate the principle of high-speed and low-speed framing operation, respectively.

The high-speed framing is performed at the line rate by using a high-speed frame detection circuit, as shown in Fig. 2. This approach is suited for detecting framing sequences that occupy a number of adjacent time slots. These bunched framing sequences are used in standard digital signals such as SONET. During the reframe (i.e., frame realignment) process, the circuit scans the outputs of the shift register and searches for a valid framing pattern. *Once a valid framing pattern is identified, the detector* will generate a frame sync pulse, FP, and set the clock divider circuit to a predetermined state so that the outputs of the demultiplexer are properly aligned. This framing approach, although conceptually simple, requires the complete frame detection circuit to operate at the line rate, and this could add considerable timing delay to the demux operation. Therefore, the conventional high-speed framing approach is not suitable for use in the gigabit/second SONET systems.

In order to maximize the performance of the line interface demux, the frame detector is often implemented at low speed as part of the receiver's parallel signal processor or tributary signal processor. Fig. 3 shows an example of low-speed framing for the SONET STS-*N* receiver. During a reframe process, the low-speed frame detector searches the parallel outputs of the demux for a valid framing pattern. If no valid framing pattern is detected, the frame detector will send a skip pulse to the demux to rotate one bit position in the demux outputs. This process will continue until a valid framing pattern is detected by the low-speed frame detector. Such an implementation usually employs separate IC's to perform the (high-speed) demultiplexing and (low-speed) frame detection functions, and this imposes stringent timing requirements on the IC's, their interfaces, and especially on the feedback control path via skip-pulse signaling. To reduce the system design complexity, we propose a new and highly efficient SONET framing scheme. This scheme is optimized for high-speed operation, and provides the natural integration of demultiplexing and SONET frame detection functions.

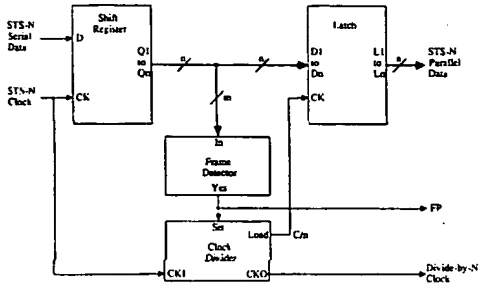

Fig. 2. Conventional high-speed demultiplexer with frame detector.

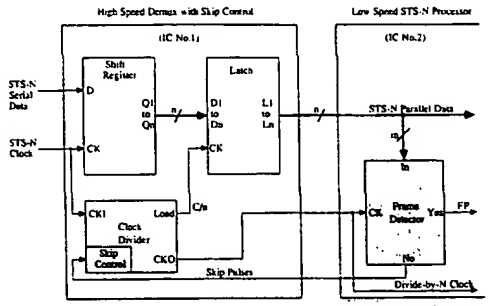

Fig. 3. High-speed demultiplexer and low-speed frame detector.

III. SONET Demultiplexing and Framing Scheme

In an STS-*N* frame, the first 2*N* bytes (*N* A1 bytes followed by *N* A2 bytes) are the SONET framing bytes. This is shown in Fig. 1, where A1 byte = 11110110, and A2 byte = 00101000. Together, these 2*N* bytes form the SONET STS-*N* framing sequence. In the new scheme, the SONET framing is accomplished in two steps: the first step is byte alignment, and the second step is frame detection. The byte alignment is a process that aligns the outputs of the demux with the data byte boundaries. This can be attained by identifying the A1 framing bytes in the STS-*N* framing sequence. The frame detection is a process that detects the STS-*N* frame boundaries from the incoming SONET signal. This is accomplished by identifying a valid framing pattern, A1A2A2, at the beginning of each STS-*N* frame. The A1A2A2 framing pattern is selected because it marks the transition from A1's to A2's in the STS-*N* framing sequence, and it can be easily detected using a simple frame detection circuit. In addition, the probability of any random data mimicking this 24 bit pattern is 2^{-24}. This ensures short (average) reframe time and infrequent false frame alignment for a gigabit/second SONET system. Note that, in the present scheme, only a few SONET framing bytes are needed for byte alignment and frame detection purposes. Therefore, this framing method can be applied to any higher level SONET signal, STS-*N*, with $N > 1$.

Fig. 4 shows the circuit block diagram of the high-speed SONET demultiplexer and framing circuitry. At the high-

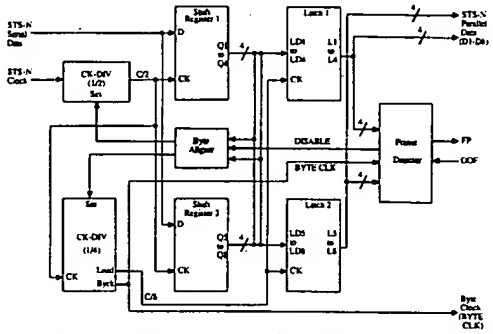

Fig. 4. High-speed SONET demultiplexer with byte aligner and frame detector.

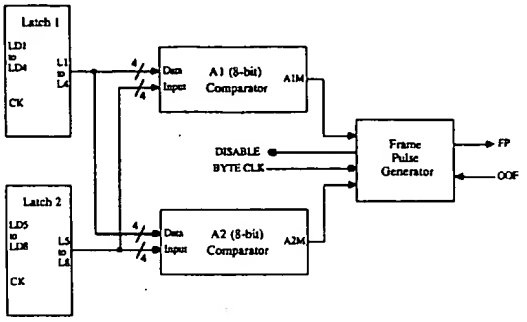

Fig. 5. SONET A1A2A2 frame detector.

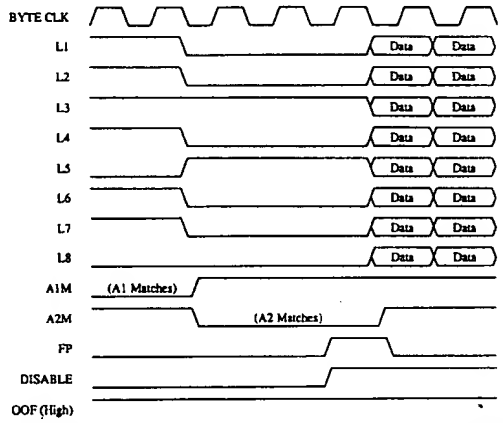

Fig. 6. Timing diagram for the A1A2A2 frame detector with a SONET STS-3 framing sequence.

speed data input, the STS-*N* signal is demultiplexed and clocked into two shift registers, 1 and 2, using the divide-by-two clock signal, C/2. Shift register 1 reads in data on the rising edge of the (C/2) clock signal, and shift register 2 reads in data on the falling edge of the (C/2) clock signal, and both registers are constructed in such a way so that their output data bit periods are carefully aligned. The outputs of the shift registers are then loaded in parallel into two 4 bit latches, 1 and 2, using the data latch timing signal, C/8. Both C/2 and C/8 are generated on-chip by using a divide-by-two (1/2) and divide-by-four (1/4) clock divider, respectively, and they are the key timing signals for controlling the demux operation. Finally, the 8-bit outputs of the data latches are sent off-chip for parallel signal processing.

During the frame recovery process, the byte aligner scans the output data of the shift registers (1 and 2), locates the A1 framing bytes, and sets the clock dividers (1/2 and 1/4) to the appropriate states so that the outputs of the data latches (1 and 2) are in byte-parallel format. The byte aligner consists of simple data comparators and flip-flops. These comparators are used to detect data patterns in the A1 framing byte, and generate the reset signals for the clock divider circuits in the demux.

Once byte alignment is accomplished, frame synchronization can be achieved by detecting the framing pattern, A1A2A2, from the demux outputs. The circuits required to perform this function include an A1 comparator, an A2 comparator, and a frame pulse generator, as shown in Fig. 5. The A1 and A2 comparators, constructed by using simple logic gates, compare the outputs of the data latches with the A1 (11110110) and A2 (00101000) framing bytes, respectively. If an A1 match followed by two consecutive A2 matches are detected, the frame pulse generator will disable the byte aligner, so that no further timing readjustment will occur in the demux. Meanwhile, the frame pulse generator will also send a frame sync pulse, FP, off-chip to synchronize the rest of the SONET receiver. Fig. 6 shows the timing diagram for the frame detector during an STS-3 frame realignment process, where BYTE CLK is the data byte clock generated by the divide-by-four clock divider, L1 to L8 are outputs of the data latches, A1M and A2M are outputs of the A1 comparator and A2 comparator, respectively, FP denotes the frame sync pulse, and DISABLE (active High) is the timing signal used to disable the byte aligner when a valid framing pattern (A1A2A2) is detected. Note that, in this figure, L1 carries the most significant bit (MSB) of a data byte, L8 carries the least significant bit (LSB) of a data byte, and the out-of-frame indicator, OOF (see below), is High throughout the frame detection period. A similar timing diagram can be generated for the SONET STS-48 reframe process.

The FP signal generated on-chip can be monitored externally by a parallel signal processor. If valid framing patterns are detected in two consecutive SONET frames, the system will declare itself "in frame," and set the OOF input on-chip to Low. This indicates that the system is in frame synchronization (or frame alignment). Once the system is in the normal in-frame state, it will have to detect at least four consecutive invalid framing patterns before it can declare itself "out of frame" (OOF). This is to ensure that the system will not experience frequent "misframes" (false out-of-frame) due to the presence of line errors (see Section IV). Fig. 7 shows an out-of-frame state diagram for a SONET system [3]. Once in the out-

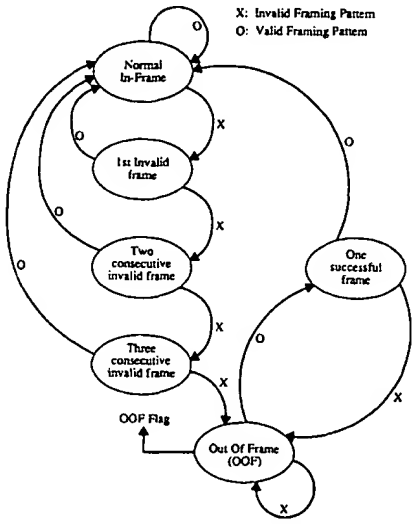

Fig. 7. Out-of-frame state diagram.

of-frame state, the external processor will assert the OOF input (Low to High) on the demux chip. This will enable the byte aligner circuit, and start the search for new SONET frames.

In the SONET demultiplexing and framing IC, only the high-speed clock-divide-by-two circuit is required to operate at the line rate. The rest of the functions, including all the framing circuitry, are designed to operate at either one half or one eighth of the line rate. Thus, the addition of small byte-alignment and frame-detection circuits will not affect the overall performance of this IC. In addition, this design greatly relaxes the timing requirements for the IC, and allows the chip designers to adopt either custom or semicustom design approaches, as long as the performance of the high-speed clock divider circuit is carefully optimized.

IV. Performance Considerations of SONET Framing Strategy

The performance of this framing strategy can be measured by two important timing parameters: the maximum average reframe time (MART) and the misframe time (MT). The maximum average reframe time is the time required to re-establish frame alignment from an inadvertent loss-of-frame (Fig. 7), assuming that the data pattern is random and the frame search starts at the worst-case position (i.e., one bit after the correct framing position). The misframe time is the mean time to declare out-of-frame due to the presence of bit errors in the framing sequence. Based on the state diagram shown in Fig. 7, one can estimate the maximum average reframe times and misframe times for the SONET receiver under different bit error rate conditions [6]. Results indicate that for a SONET STS-48 receiver with a transmission bit error rate of 10^{-3}, the maximum average reframe time is approximately $2.08T$, where T is the period of a SONET frame (125 μs). For a bit error rate of 10^{-6}, the MART becomes $2.01T$. The corresponding values for an STS-12 receiver are about $2.08T$ and $2T$, respectively. The misframe times at 10^{-3} and 10^{-6} bit error rates are estimated to be around 6.3 minutes and 1.1×10^{7} years, respectively. These numbers indicate that the new SONET framing scheme provides fast reframe times and long misframe times even in very high bit-error-rate conditions.

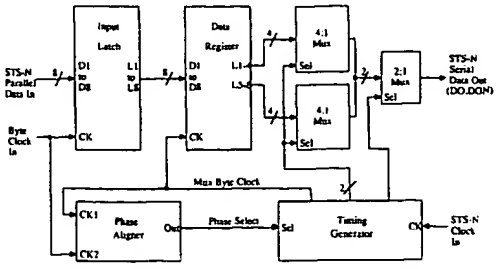

Fig. 8. High-speed multiplexer with phase aligner.

V. High-Speed Multiplexer Design

A high-speed multiplexer IC was designed for the SONET STS-48 line interface circuit. This IC can also be used to interface at any other SONET signal level. Fig. 8 shows a circuit block diagram of the IC. The 8:1 multiplexing function is divided into two stages, a high-speed 2:1 stage and a low-speed 4:1 stage. The timing signals required for the multiplexer are generated by a timing generator. On the low-speed side, the input data bytes are clocked on-chip by using an "input byte clock." In a SONET transmitter, this "input byte clock" is synchronous (in frequency) with the "mux byte clock," but they are generally out of phase alignment. To ensure that the parallel input data are properly latched and multiplexed, a phase aligner circuit is implemented on-chip. This circuit performs a phase comparison between the "input byte clock" and the "mux byte clock," and then generates a phase select signal to select the proper phases for the mux timing generator. The high-speed output of the multiplexer is a serial signal at the STS-48 data rate. This two-stage circuit design minimizes the amount of high-speed circuitry required to run at the STS-48 line rate, thereby relaxing the timing constraints on the IC.

A separate 8:1 multiplexing scheme has also been implemented for the IC. This scheme employs multiple 2:1 data selectors connected to form a three-stage (8:1) multiplexing tree. Both the two-stage and three-stage architectures are suitable for use in the gigabit/second SONET multiplexer.

VI. Circuit Implementation and Test Results

The SONET prototype IC's were implemented using a 1 μ GaAs enhancement/depletion (E/D) MESFET structured cell array [7]. There are three types of active devices

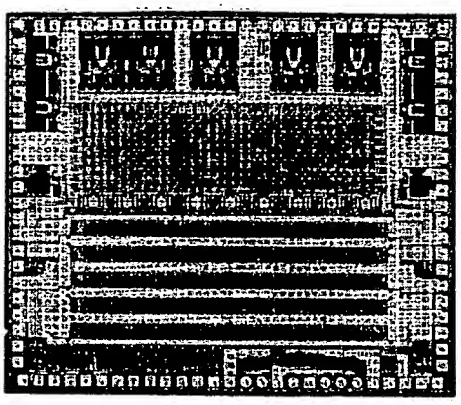

Fig. 9. Microphotograph of the SONET demultiplexer chip.

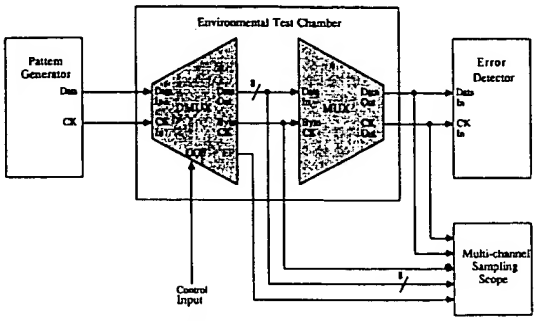

Fig. 10. Experimental setup.

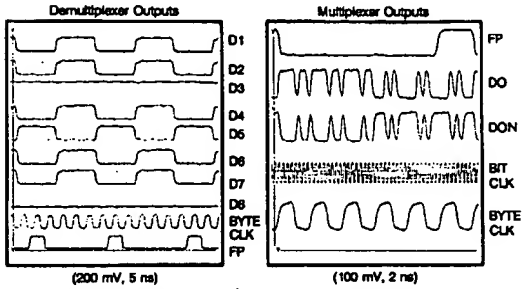

Fig. 11. SONET multiplexer and demultiplexer output waveforms at the STS-48 rate of 2.488 Gb/s. The picture on the left shows the demultiplexer outputs, i.e., parallel data (D1-D8), byte clock (BYTE CLK), and frame sync pulse (FP). The picture on the right shows the multiplexer outputs, DO and DON. Also shown on the right are frame sync pulse (FP), bit clock (BIT CLK), and byte clock (BYTE CLK). For display convenience, a repeated STS-3 framing sequence (A1A1A1A2A2A2) is used instead of the actual STS-48 signal.

Fig. 12. Multiplexer output eye diagram at 2.8 Gb/s data rate.

in the circuits: the enhancement mode MESFET's, the depletion mode MESFET's, and the Schottky barrier diodes. The transistors are used both as switching elements and as active loads, and the Schottky barrier diodes are used primarily for level shifting between circuit elements, such as gates, flip-flops, etc. To attain a good performance for the high-speed circuitry, an ECL-like logic called SCFL (source-coupled FET logic) is employed. These circuits are fully differential, and they are carefully optimized to ensure proper operation at the STS-48 rate. The low-speed sections, operating at one eighth of the line rate, are implemented using the low-power DCFL (direct-coupled FET logic) circuits, and an array of translation cells is used to provide logic level translation between the SCFL and DCFL circuits. All the data and clock inputs and outputs (I/O's) on the mux and demux chips are differential. In addition, both IC's employ ECL-compatible 8-bit-wide data I/O's and power supplies (V_{EE} = −5.2 V, V_{TT} = −2 V). Fig. 9 shows a microphotograph of the SONET demultiplexer IC. The upper half of the photograph shows the high-speed SCFL circuitry, the lower half of the photograph shows the DCFL circuitry, and the translation cells are situated between the SCFL and DCFL circuit blocks. The IC contains approximately 2300 devices on a 3.5 × 4 mm die, dissipates about 2.5 W of power, and has an estimated yield of around 50%.

The SONET prototype IC's are housed in 52-pin leaded ceramic chip carrier packages. The multiplexer and demultiplexer (with byte aligner and frame detector) were tested in a back-to-back configuration. Fig. 10 depicts the experimental test setup. In this configuration, the serial data and clock inputs of the demultiplexer are connected to a high-speed pattern generator, and the parallel data and byte clock outputs of the demultiplexer are connected to the parallel data and byte clock inputs of the multiplexer. The outputs of the IC's are sent to a multichannel sampling scope and an error detector to perform waveform analyses and bit error rate measurements, respectively. Results indicated that the experimental prototype SONET demultiplexer IC can detect SONET STS-3 to STS-48 framing sequences. In addition, both the multiplexer and demultiplexer IC's can operate over a wide frequency range from 10 MHz to 3 GHz. Fig. 11 shows the demux output waveforms, including data (D1-D8), byte clock, frame sync pulse (FP), and the multiplexer output waveforms, i.e., STS-N serial data out (DO, DON), at 2.488 Gb/s. For display convenience, a repeated STS-3 framing sequence (A1A1A1A2A2A2) is used in the figure instead of the actual STS-48 signal. Note that, for each valid framing pattern detected (see waveforms D1-D8), an FP pulse is generated by the demux. Fig. 12 shows the multiplexer output eye diagram at 2.8 Gb/s. Bit error rate tests were performed for the mux and demux IC's at 2.488 Gb/s using a $2^{23} - 1$ pseudorandom

NRZ sequence. Results indicated that the IC's can function properly at this speed with a bit error rate less than 10^{-14}. The power supply tolerance for these tests was about 10% (−5.46 ~ −4.94 V).

VII. Conclusion

An experimental GaAs SONET multiplexer and demultiplexer chipset has been prototyped. The demultiplexer IC contains a two-stage 1 : 8 demux, a byte aligner, and a SONET frame detector. The IC was designed to minimize the amount of high-speed line-rate circuitry, and it allows an easy integration of the demultiplexing and framing functions. The novel framing circuits operate from the STS-3 (155.52 Mb/s) to the STS-48 (2.488 Gb/s) rates, and provide fast reframe times even under very high bit-error-rate (e.g., 10^{-3}) conditions. The multiplexer IC contains an 8 : 1 mux and a phase aligner, and the bit error rate test results show that the multiplexer and demultiplexer with framing circuits can operate at 2.488 Gb/s with a total bit error rate less than 10^{-14}. Both IC's were tested at data rates up to 3 Gb/s. This performance demonstrates the feasibility of using GaAs IC's in SONET and broadband applications where high speed, high yield, and high functional integration are required.

Acknowledgment

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